HYBRID MULTIPLIERS IMPLEMENTED USING DSP CIRCUITRY AND PROGRAMMABLE LOGIC CIRCUITRY

Abstract of the Invention

[0065] A user logic design to hardware application is provided that efficiently implements in a PLD a user logic design multiplier using both programmable logic circuitry and one or more multipliers embedded in DSP circuitry integrated in the PLD. A smaller DSP multiplier may be used by implementing the user logic design multiplier in a sum of partial product arrangement in which one of the partial products is generated using the smaller DSP multiplier with the remaining partial products being generated by multipliers implemented using programmable logic circuitry.